Lecture Time and Place
TuTh 3:00p.m. - 5:20p.m. in Room 123 Chemistry Building

Prerequisite
ESE 305 and ESE 380. Students are expected to know the logic design, digital circuits, signals and systems, and some programming. Some background in computer architecture is helpful but not required.

Textbook

Course Goals
This course covers various aspects of architectures in digital signal processing and multimedia data processing. The topics include iteration bound analysis, retiming the circuits, unfolding and folding the architectures, algorithmic and numerical strength reduction for low power and low complexity design, introduction to array processor architectures and CORDIC implementation.

Project
This is a project-oriented course. No specific lab times are scheduled, and you can work at your convenience.

Course Contents
Week 1: Course Overview, Circuits and Systems
Week 2: Algorithm Representation
Week 3: Iteration Bound and Analysis
Week 4: Retiming, Clock Minimization
Week 5: Register Minimization, Complexity Reduction
Week 6: Unfolding, Parallelization
Week 7: Folding, Bit Serial Architecture
Week 8: Folding, Complexity Reduction
Week 9: Numerical Strength Reduction, CSD
Week 10: Array Processor, Systolic Architecture
Week 11: 3-D Systolic Architecture
Week 12: Algorithm Strength Reduction
Week 13: Scaling and Round-Off Noise
Week 14: Advanced Topics

**Grading**

The grading will be based upon:
1. 6 Homework Assignments (20%)
2. 1 Project (30%)
3. 2 Midterm Exams (50%)

**Blackboard**

You can access class information on-line at: http://blackboard.stonybrook.edu
For help see: http://it.stonybrook.edu/services/blackboard
For problems logging in, go to the helpdesk in the Main Library SINC Site or the Union SINC Site; you can also call: 631-632-9602 or e-mail: helpme@stonybrook.edu

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