ESE 566: Hardware/Software Co-Design of Embedded Systems
Fall 2016

Instructor: Dr. Alex Doboli.
Credits: 3 credits
Schedule: TBD.

Description: The course presents state-of-the-art concepts and techniques for design of embedded systems consisting of analog, hardware and software components. Discussed topics include system modeling and specification, architectures for embedded mixed-signal systems, performance evaluation, and system optimization. The course follows the top-down design paradigm based on IP cores. Course requirements include three reports on system specification and various co-design tasks.

Goal: Upon completion of the course, students will possess knowledge about state-of-the-art methodologies and techniques for hardware/software co-design of embedded systems. They will be able to (1) develop system-level specifications using high-level languages, (2) model system performance, and (3) implement algorithms for co-design.

Text Book and other Teaching Material:

Other Material:
3. Other published papers will be provided in class.

Prerequisites: ESE 545 (Computer Architectures), ESE 554 (Computational Models), and ESE 333 (Real-Time Operating Systems) or equivalent. Upon request, the instructor might waive the prerequisites.

Covered Topics:
1) Introduction to Co-Design:
   a. Problem description, goals of co-design, co-design steps, existing co-design approaches, and present challenges.

2) System Modeling and Specification:
   a. Models of computation (Signal flow graphs, Data flow model, Task graphs, Finite State Machines, hierarchical models).

3) Architectures for Embedded Systems:
   b. Report 1 on embedded mixed-signal architectures.

4) Performance Modeling:
   b. Modeling of system latency, energy consumption etc for hardware and software.
   c. Modeling of analog and mixed-signal systems.
   d. Estimation of memory requirements.
5) **System-Level Synthesis and Trade-off Analysis:**
   a. Design of customized digital and analog blocks.
   b. Hardware/software partitioning. Task binding.
   c. IP core integration and communication synthesis: Hardware and software interface synthesis.
   d. Hardware IP core synthesis: High-level synthesis: behavioral specification of hardware, module set allocation, resource binding, operation scheduling, controller design.
   e. Reports 2 and 3 on various embedded design tasks.

**Other Course Material:**
1) Other relevant papers will be provided in class.

**Grading:**
Final grade = 0.25 Report₁ + 0.25 Report₂ + 0.25 Midterm + 0.25 Final

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