EEO 219: Digital Logic Design Laboratory

Fall 2016

2016-2017 Catalog Description:

The digital circuits are designed and simulated with CAD tools, assembled on a breadboard and verified with a logic analyzer.

Course Designation: Required Course

Text Book: none

Prerequisite or co-requisite: EEO218

Credit Hours: 1
Coordinator: Dmitri Donetski
Goals: Development of practical skills necessary for taking advanced Electrical and Computer Engineering courses.

Course Learning Outcomes: Upon completion of the course, students will have

- skills in reading schematic of digital circuits and analysis of circuit behavior;
- skills in design of combination and sequential circuits using conventional methods and CAD tools;
- skills in verification and troubleshooting circuits with a logic analyzer, determination of signal propagation delays.

Topics Covered:

Week 1.	No lab
Week 2.	No lab
Week 3.	Lab 1. Breadboard and Logic analyzer. Logic gate propagation delays, ring oscillator, effect of capacitive load.
Week 4.	Lab 2. Algebraic manipulations: multilevel, NAND-NAND, NOR-NOR implementations. Alarm circuit.
Week 5.	Lab 3. Static glitches in 2-level implementations. 2-to-1 multiplexer.
Week 6.	Lab 4. Code converter: incompletely specified functions, hierarchical design, buses.
Week 7.	Lab 5. Binary adder/subtractor for signed integers with overflow detection.
Week 8.	Lab 6. Instruction decoder. Implementation of switching functions with decoders.
Week 9.	Lab 7. Comparator of 2-bit numbers. Implementation of switching functions with multiplexers.
Week 10.	Lab 8. Generator of 2-phases ynchronization signals. Flip-flops. Clock

	divider. Glitches and glitch-free design.
Week 11.	Lab 9. Counter. Design of finite state machines with D-flip-flops and mutliplexers.
Week 12.	Lab 10, week 1. Serial communications. Data scrambler based on linear feedback shift register. Controller design for the datapath.
Week 13.	Lab 10, week 2. Serial communications. Cyclic redundancy check (CRC-3). Controller design for the datapath.
Week 14	Lab 11. Sequential binary multiplier. Datapath and controller desing.

Class/laboratory Schedule: 3 lab hours per week, students will spend additional time on prelabs.

Student Outcomes	**% contribution***
(a) an ability to apply knowledge of mathematics, science and engineering	10
(b1) an ability to design and conduct experiments	20
(b2) an ability to analyze and interpret data	20
(c) an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability	20
x (d) an ability to function on multi-disciplinary teams	
(e) an ability to identify, formulate, and solve engineering problems	10
x (f) an understanding of professional and ethical responsibility	
x (g) an ability to communicate effectively	
x (h) the broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context	
(i) a recognition of the need for, and an ability to engage in life-long learning	
(j) a knowledge of contemporary issues	
(k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice	20
Any other outcomes and assessments?	

* Assume that the total contribution of any course will be 100%. Use the right hand column to indicate the approximate percent that the left hand columns contribute to the overall course.

Document Prepared by: Dmitri Donetski
Date: May 2017