EEO 218: Digital Logic Design

Fall 2016

2016-2017 Catalog Description:

The course covers binary numbers, Boolean algebra, arithmetic circuits, flip-flops, analysis and design of sequential circuits, memory and programmable logic.

Course Designation: Required Course

Text Books: M. Morris Mano, Michael D. Ciletti, "Digital Design", 5th ed., Prentice Hall, 2013, ISBN-13: 978-0-13-277420-8, ISBN-10: 0-13-277420-8

Prerequisites: Physics II

Credit Hours: 3

Coordinator: Dmitri Donetski

Goals: Development of general background necessary for taking advanced Electrical and Computer Engineering courses.

Course Learning Outcomes: Upon completion of the course, students will have

- understanding fundamentals of analysis and design of digital circuits and standard building blocks;
- skills in reading schematic of digital circuits and analysis of circuit behavior;
- skills in design of combination and sequential circuits using conventional methods.

Topics Covered:

Week 1.	Binary numbers, base conversion, conversion error. Number formats. Addition in binary, subtraction by addition of a 2's complement. Logic operations and gates. CMOS fabrication technology.
Week 2.	Boolean algebra. Duality principle. BCD, 10's complements. Unicodes, Gray codes. Error detection and correction. Parity, distance, CRC, Hamming codes.
Week 3.	Pass transistor logic, dynamic logic. Propagation delay, transition time, fan–in, fan–out, buffering. Standard forms. Two-level implementations. AOI, OAI. Minimization and form conversion., consensus. Test signals, waveforms, critical path, race conditions, static glitches. Incompletely specified functions.
Week 4.	Decoders: implementation of switching functions, enable, predecoding. Encoders. Multiplexers. Transmission gate, implementation of switching functions, barrel shifters. Introduction to Hardware Description Languages.
Week 5.	Review for test 1. Problem solving.
Week 6.	Half adder, full adder. CMOS and PTL 1-bit adders. Carry generate, propagate, kill. Incrementer, decrementer. Subtractors, overflow detection. RCA, CLA, CSA. Inversion property. Array multiplier.
Week 7.	SR- and D-latches. Critical racing. Metastability. Setup time, hold time, propagation delay. CMOS Master-slave D-flip-flop. Asynchronous Preset and Clear. JK-, T-flip-flops. State tables, state diagrams, characteristic equations.
Week 8.	Analysis and design of synchronous finite state machines with D-flip-flops. Mealy and Moore outputs. Max clock frequency. Frequency dividers, parity bit checker, edge detectors, synchronizers, sequence detectors

Week 9.	Binary counters with D–and T-flip-flops. Counters with Preset. Registers. Blocking vs non-blocking assignments. Register-based counters. Ring and Johnson counters, hang-up states, state decoding.
Week 10.	Asynchronous circuits. Ripple counters. LFSR, PRNG, data scrambling, CRC-3. Serial data transfer, SPI, I2C.
Week 11.	Review for test 2. Problem solving.
Week 12.	RTL, operations, datapath, controller, ASM and ASMD charts. Sequential multipliers. State assignment. State reduction, implication chart, partitioning.
Week 13.	Flash ROM, NAND vs NOR. SRAM, DRAM, refreshing, bandwidth and latency. DDR. Programmable logic. MCPLD vs FPGA, logic, RAM, I/O blocks.
Week 14	Review for the final exam

Class/laboratory Schedule: 2h 40 min lecture hours per week, students will spend additional time on 11 homeworks.

Student Outcomes	**% contribution***
(a) an ability to apply knowledge of mathematics, science and engineering	20
(b1) an ability to design and conduct experiments	
(b2) an ability to analyze and interpret data	
(c) an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability	40
x (d) an ability to function on multi-disciplinary teams	
(e) an ability to identify, formulate, and solve engineering problems	40
x (f) an understanding of professional and ethical responsibility	
x (g) an ability to communicate effectively	
x (h) the broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context	
(i) a recognition of the need for, and an ability to engage in life-long learning	
(j) a knowledge of contemporary issues	
(k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice	
Any other outcomes and assessments?	

* Assume that the total contribution of any course will be 100%. Use the right hand column to indicate the approximate percent that the left hand columns contribute to the overall course.

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